ZingSom2

Embedded Processing Module

User Manual

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Document History

Version	Date	Author	Comment
0.9	19.11.2014	V3Best	First draft

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1 Overview

1.1 General

The ZingSom2 embedded processing module combines Xilinx' Zynq-7000 Extensible Processing Platform (EPP) device with fast DDR3 SDRAM, NAND flash, a Gigabit Ethernet PHY and thus forms a complete and powerful embedded processing system. The SO-DIMM form factor allows space-saving hardware designs as well as quick and simple integration of the module into the target application. The ZingSom2 Embedded Processing module reduces development effort, redesign risk and improves time-to-market for your embedded system.

The use of ZingSom2 EPP modules, in contrast to building a custom EPP hardware, significantly simplifies system design and thus shortens time to market and decreases the development effort of your product.

The ZingSom2 Starter base boards enable you to quickly put together a prototyping system and start developing your system 'hands-on'.

1.2 Features

- Xilinx Zynq-7020 EPP in the CLG400 package
  - Dual ARM® Cortex™-A9 MPCore™ with CoreSight™ and NEON™ extension running at up to 800 MHz
  - Artix-7 28 nm FPGA fabric as programmable user logic
- Up to 512MB DDR3 SDRAM
- Up to 8 Gb NAND Flash
- Gigabit Ethernet PHY
- USB 2.0 OTG PHY
- 33.333 MHz Oscillator
- user I/Os
- Single 3.3 V supply
- SO-DIMM form factor: 200 Pins, 30 x 68 mm

1.3 Deliverables

Standard deliverables:

- ZingSom2 embedded processing module
- ZingSom2 user manual (this document)
- ZingSom2 pinout list (Microsoft Excel document)

1.4 ZingSom2 Starter Board

- ZingSom2 SO-DIMM socket
- JTAG
- HDMI Port
- VGA Port
- RS232 Uart
- Micro USB Uart
- Audio Port
- 2x PMOD-Connector
- RJ45 Ethernet connector
- MicroSD Card holder
- Various switches and LEDs
- Single 6 V supply
- Form factor: 160 x 80 mm
- Mode select switches

2 Module Description

2.1 Block Diagram

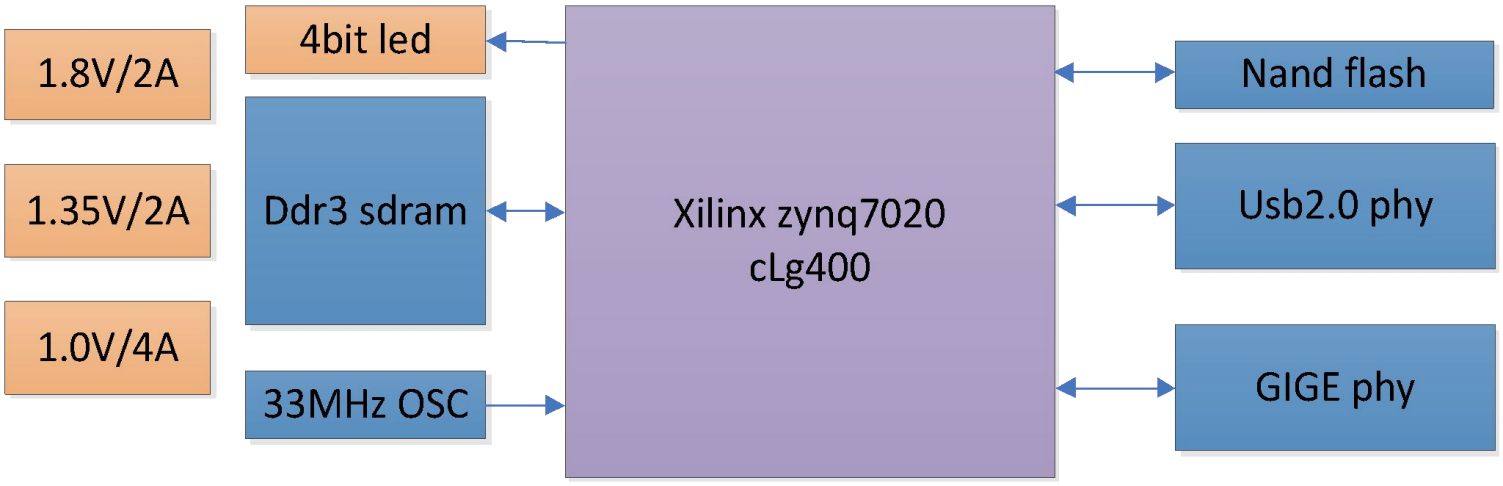

Figure 1: Hardware Block Diagram

The heart of the ZingSom2 embedded processing module is the Zynq-7000 EPP device. Most of its I/O pins are connected to the ZingSom2 module connector, making user I/Os available at the ZingSom2 module connector.

The available standard configurations include 4 Gb NAND Flash and 256 or 512 MB DDR3 SDRAM.

The Zynq-7000 EPP device is either configured with an image residing in the TF Card or Nand Flash via an external microcontroller or via the JTAG interface connected to the ZingSom2 module connector.

The module is also equipped with a gigabit Ethernet PHY and a USB 2.0 OTG PHY, making it ideal for embedded and communication applications.

Clock generation is done by a 33 MHz crystal oscillator. The module can be supplied by a single 3.3 V power supply.
Four LEDs are connected to the EPP pins for easy status signaling.

2.2 Module Configurations

Table 1 shows the available module configurations. Custom configurations are possible; please contact us for further information.

Part number	EPP	DDR3 SDRAM	NAND Flash	Temp Range
ZingSom2	XC7Z020-1CCLG400C	512MB	4Gb	-40----85°C

Table 1: Available Module Configurations

2.3 Top-/Bottom Views

2.3.1 Top View

Figure 2: Module Top View

2.3.2 Bottom View

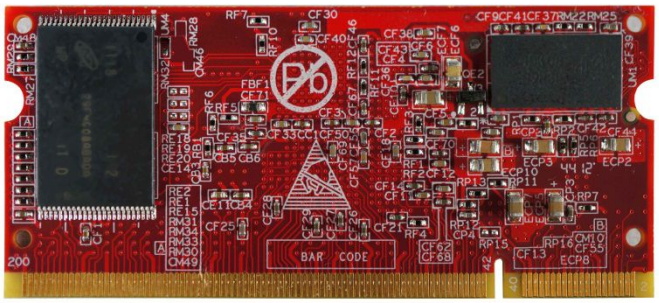

Figure 3: Module Bottom View

2.4 ZingSom2 Module Connector

The ZingSom2 fits into a 200 pin DDR2-SODIMM (1.8 V) socket. The pinout of the module connector is found in Appendix A.

Table 2 shows some matching connector types in different heights.

Table 2: ZingSom2 Module Connector Types

Height	Type	Description	Max component height under the module

4.0 mm	Tyco 292406	DDR2-SODIMM, 1.8 V	0 mm
5.2 mm	FCI 10033853	DDR2-SODIMM, 1.8 V	1 mm
6.5 mm	Tyco 1746530	DDR2-SODIMM, 1.8 V	2 mm
8.0 mm	Tyco 1747407	DDR2-SODIMM, 1.8 V	4 mm

2.5 Power

2.5.1 Power Generation Overview

The ZingSom2 embedded processing module uses a VCC_IN(3.3V) power input for generating the three on- board supply voltages (1.0 V, 1.35 V, 1.8 V). These internally generated voltages are also accessible on the module connector. In addition, a separate 3.3 V power input is present to supply peripherals like Ethernet PHY, Flash, Oscillator and LEDs.

2.5.2 Power Enable

The ZingSom2 embedded processing module provides a power enable input on the ZingSom2 module connector. This input may be used to shut down the DC/DC converters for 1.0 V, 1.35 V and 1.8 V, which leaves the EPP and the DDR3 SDRAM unpowered. It will also detach the separate 3.3 V power input from the peripherals.

The PWR_EN input is pulled to 3.3 V on the ZingSom2 embedded processing module with a 4.7k pull- up resistor. Leaving it unconnected will thus result in a constantly powered EPP.

The PWR_GOOD signal is pulled to 3.3 V on the ZingSom2 embedded processing module with a 49.9k pull-up resistor. The signal is pulled to GND if any of the on board regulators (1.5 V or 1.8 V) fail. Table 3 shows the module power enable pins

Table 3: Module Power Enable Pins

Pin Name	Module Connector Pin	Remarks
PWR_EN	13	Floating/3.3 V: EPP power enabled Tied to GND: EPP power disabled
PWR_GOOD	40	0: EPP supply not ok 1: EPP supply ok

2.5.3 Supply Voltage Inputs

A total of three supply voltages exist on the ZingSom2 module. All of them may be connected to a single 3.3 V supply. Table 4 shows the supply voltage inputs.

Table 4: Supply Voltage Inputs

Pin Name	Module Connector Pins	Voltage	Description
VCC_IN	1, 3, 5, 7, 9, 11	3.3V	Supply for the 1.0 V, 1.35 V and 1.8 V regulators
3.3V	197, 199	3.3V	Supply for Ethernet PHY, Flash, Oscillator and LEDs
FPGA_VBATT	200	1.65V	Battery for EPP encryption key.

2.5.4 Supply Voltage Outputs

Three of the supply voltages generated on the ZingSom2 are available on the ZingSom2 Module Connector. Table 5 shows supply voltage outputs

Table 5: Supply Voltage Outputs

Pin Name	Module Connector Pins	Voltage
1.0V	42	1.0 V +/- 5%
1.35V	41	1.35 V +/- 5%
1.8V	89, 94, 101, 106	1.8 V +/- 5%

2.6 Analog Inputs

The EPP devices contain a dual 12bit ADC. The analog inputs of the EPP device are connected to the ZingSom2 Module connector. These IOs have the abbreviation "AD" followed by the ADC channel in the signal name, e.g. IO_B35_L5P_**AD9P**_F18 and IO_B35_L5N_**AD9N**_E18. The two dedicated ADC pins VP and VN are also available on the module connector (Pins 168 and 170).

The ADC can also be used for internal voltage and temperature monitoring. For more details please refer to the Zynq technical reference manual.

The ADC lines are always used differentially. For single-ended applications the _N line has to be connected to GND. Table 6: ADC parameters

Table 6: ADC parameters

Parameter	Value
VCC_ADC	1.8V
VREF_ADC	1.25V
ADC Range	0—1V
Sampling rate per ADC	1MSPS
Total number of channels	16

2.7 Clock Generation

A 33.333 MHz crystal oscillator is connected to the EPP device. Figure 4 shows the clock source circuit.

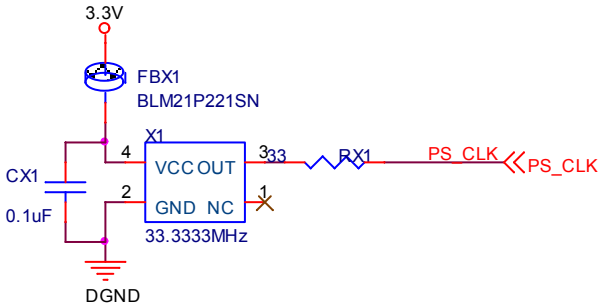

Figure 4: Clock Source Circuit

Table 7 shows the clock resources.

Table 7: Clock Resources

Signal Name	Freq(MHz)	EPP Pin	EPP Pin Type
PS_CLK	33.333	E7	PS_CLK

2.8 Reset

The power on reset (POR) of the EPP device is available on the ZingSom2 module connector. Other ZingSom2 modules have the FPGA_PROG_N pin connected to this pin.

Pulling PS_POR# low resets the EPP device as well as the Ethernet and the USB PHYs. The FPGA part keeps its configuration but since the EPP is hold in reset, the internal clocks will be disabled. The PS_POR# has an on-board 10k pull-up resistor. Table 8 shows the reset resources.

Table 8: Reset Resources

Signal Name	Connector Pin	EPP Pin	EPP Pin Type	Description
PS_POR#	196	C7	PS_POR_B	Hard Reset
PS_SRST#	192	B10	PS_SRST	Soft Reset

2.9 LEDs

2.9.1 EPP LEDs

Four LEDs are connected to the EPP. Please see Figure 5 to locate them on the module hardware.

Figure 5: EPP Leds

Table 9 shows the EPP leds description.

Table 9: EPP LEDs

Signal Name	EPP Pin	EPP Pin Type	Remarks
LEDG0	R19	IO_0_34	Active low
LEDG1	T19	IO_25_34	Active low
LEDG2	G14	IO_0_35	Active low
LEDG3	J15	IO_25_35	Active low

2.10 DDR3 SDRAM

The equipped DDR3 SDRAM runs at up to 533 MHz (CL 7-7-7) and is organized in 8 banks. Two chips are connected in parallel to achieve 32bit data with. Figure 6 shows one of the two chips.

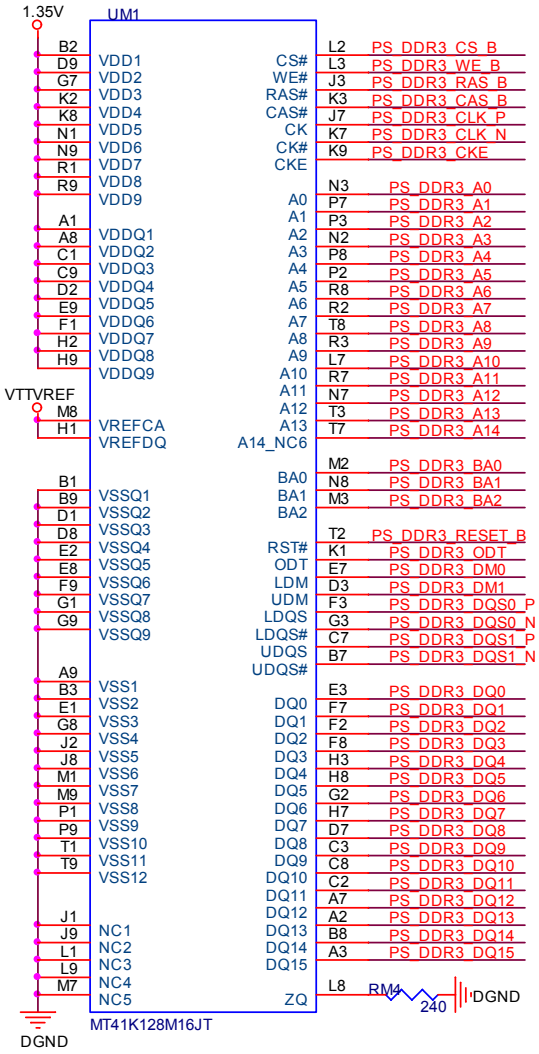

Figure 6: DDR3 Sdram Circuit

2.10.1 DDR3 SDRAM Type

Table 10 shows the equipped DDR3 SDRAM types.

Table 10: DDR3 SDRAM Type

Type	Size	Configuration	Manufacture
MT41J128M16JT	256MB	128M x 16bit	Micrel

2.10.2 Signal Description

Please refer to the ZingSom2 embedded processing module pinout sheet for detailed information about the DDR3 SDRAM connections.

2.10.3 Configuration

No external termination is implemented on the hardware. It is thus strongly recommended to enable the DDR3 SDRAM device's on-die termination (ODT) feature.

The chip select is always active, use the clock enable signal to disable the device if not used.

2.10.4 Parameters

Table 11 shows DDR3 SDRAM Parameters.

Table 11: DDR3 SDRAM Parameters

Parameter	Value
Memory Type	DDR3
DRAM Bus Width	32 bit
Operating Freq	533 MHz
DRAM IC Bus width	16 bits
Device Capacity	1024 bits
Speed Bin	DDR3_1066
Bank Bits	3
Row Bits	14
Column Bits	10
CAS latency	7
CAS write latency	6
CAS to RAS delay	4
Precharge time	6
tRC	49.5 ns
tRASmin	36 ns
tFAW	45 ns

2.11 Flash

The NAND Flash can be used to store the FPGA bitstreams, ARM application code (e.g. the bootloader) and other user data. It is connected to the EPP MIO port and the signals are also available on the ZingSom2 module connector.

Figure 7 shows the circuits of NAND flash .

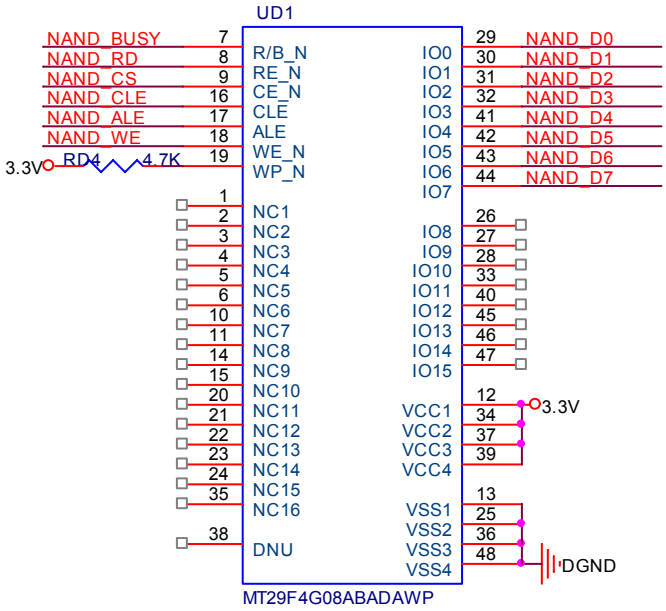

Figure 7: NAND Flash Circuit

Please refer to section 3 for more details about programming the Flash memory.

2.11.1 Flash Type

Table 12 shows the equipped Flash device type.

Table 12: Flash Type

Flash Type	Chip Type	Size
NAND Flash	MT29F4G08ABADAWP	4Gb

2.11.2 Signal Description

Table 14 shows the signals of the NAND Flash interface.

Table 14: SPI Flash Signal Description

Signal Name	EPP Pin	ZingSom2 Connector Pin	IO Voltage
NAND_CS	E6 / MIO0	-	3.3V
NAND_ALE	B8 / MIO2	-	3.3V
NAND_WE	D6 / MIO3	184	3.3V
NAND_D2	B7 / MIO4	186	3.3V
NAND_D0	A6 / MIO5	188	3.3V
NAND_D1	A5 / MIO6	190	3.3V
NAND_CLE	D8 / MIO7	-	3.3V
NAND_RD	D5 / MIO8	182	3.3V
NAND_D4	B5 / MIO9	-	3.3V
NAND_D5	E9 / MIO10	-	3.3V
NAND_D6	C6 / MIO11	-	3.3V

NAND_D7	D9 / MIO12	-	3.3V
NAND_D3	E8 / MIO13	-	3.3V
NAND_BUSY	C5 / MIO14	-	3.3V

2.12 Ethernet

There is one 10/100/1000 Mbit Ethernet PHY on the ZingSom2 board, connected to the EPP via the RGMII interface.

The RGMII interface is connected to the MIO port for use with the integrated MAC.

The Ethernet signals on the ZingSom2 Module connector can be connected directly to the magnetics. The center tap voltage is also provided by the ZingSom2 embedded processing module. The LED signals are active low. Figure 9 shows the Ethernet PHY circuit

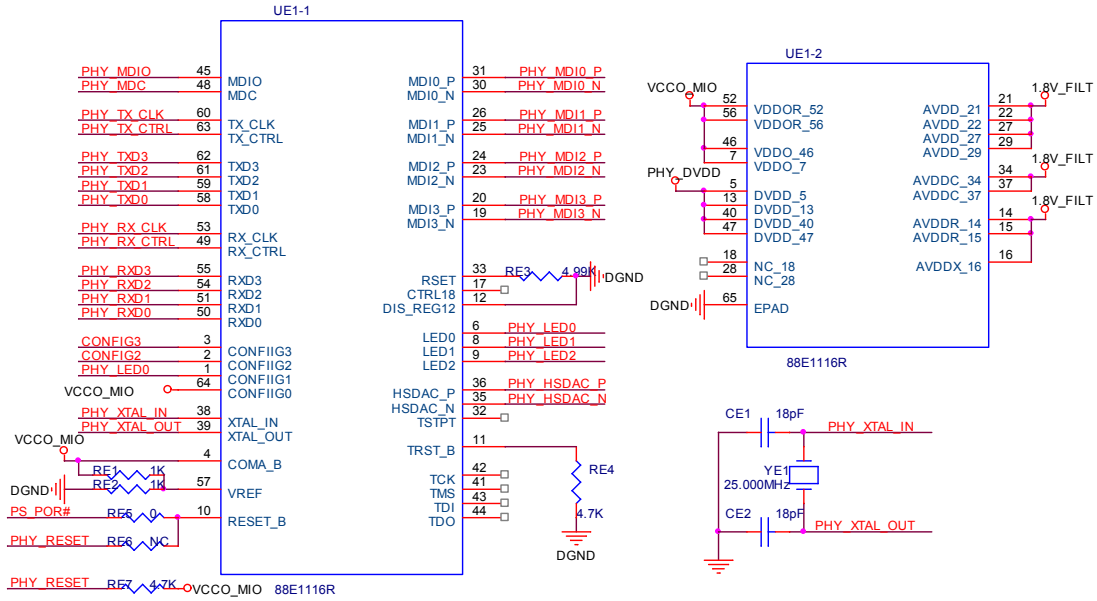

Figure 9: Ethernet PHY Circuit

2.12.1 Ethernet PHY Type

Table 15 shows the equipped Ethernet PHY device type.

Table 15: Ethernet PHY Type

Module	Type	Manufacturer	Type
ZingSom	88E1116R	Marvell	10/100/1000 Mbit

2.12.2 MDIO Address

The PHY uses address 3 on the MDIO bus.

2.12.3 Signal Description

Table 16 shows the ethernet signal description.

Table 16: Ethernet Signal Description

XC7Z020 EPP	Signal Name	88E1116R PHY(UE1-1)

Pin Name	Bank	Pin Number		Pin Number	Pin Name
PS_MIO53	501	C11	PHY_MDIO	45	MDIO
PS_MIO52	501	C10	PHY_MDC	48	MDC
PS_MIO16	501	A19	PHY_TX_CLK	60	TX_CLK
PS_MIO21	501	F14	PHY_TX_CTRL	63	TX_CTRL
PS_MIO20	501	A17	PHY_TXD3	62	TXD3
PS_MIO19	501	D10	PHY_TXD2	61	TXD2
PS_MIO18	501	B18	PHY_TXD1	59	TXD1
PS_MIO17	501	E14	PHY_TXD0	58	TXD0
PS_MIO22	501	B17	PHY_RX_CLK	53	RX_CLK
PS_MIO27	501	D13	PHY_RX_CTRL	49	RX_CTRL
PS_MIO26	501	A15	PHY_RXD3	55	RXD3
PS_MIO25	501	F15	PHY_RXD2	54	RXD2
PS_MIO24	501	A16	PHY_RXD1	51	RXD1
PS_MIO23	501	D11	PHY_RXD0	50	RXD0

MIO52 and MIO53 can be used for MDIO or I2C.

2.12.4 PHY Clock Source

A 25.00 MHz 50 ppm crystal at YE1 is the clock source for the 88E1111 PHY at UE1. Figure 10 shows the clock source.

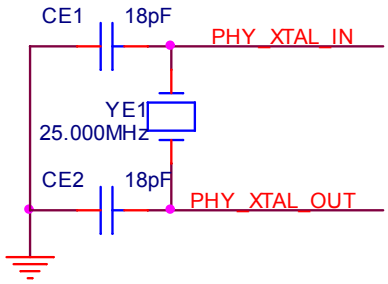

Figure 10: PHY Clock Source

3 Device Configuration

Table 17 shows the configuration pins and their location on the ZingSom2 module connector.

Table 17: EPP Configuration Interface

Signal Name	EPP Pin	EPP Pin Type	SPI Flash Pin	ZingSom2 Connector Pin
FPGA_DONE	T12	DONE_0	-	194
PS_SRST#	C9	PS_SRST#	-	192
PS_POR#	B5	PS_POR#	-	196

3.1 Flash Programming

The signals of the Flash are directly connected to the module connector. Because the Flash signals are also connected to the EPP device, the EPP pins must be tri-stated while accessing the Flash directly.

3.2 JTAG

The ARM and FPGA JTAG interfaces are connected to a single JTAG chain. This interface can be used to debug the ARM processor as well as to configure and debug the FPGA logic.

3.2.1 Signal Description

The JTAG pins of the EPP are connected directly to the module connector. Table 29 shows the JTAG interface.

Table 29: JTAG Interface

Signal Name	EPP Pin	EPP Pin Type	ZingSom2 Module Connector Pin
JTAG_TCK	F9	TCK	158
JTAG_TMS	J6	TMS	162
JTAG_TDI	G6	TDI	160
JTAG_TDO	F6	TDO	164

3.2.2 External Connectivity

Figure 11 shows the external connectivity of the JTAG connector for use with the Xilinx platform cable USB. No pull-up/down resistors are necessary.

The EPP may be configured conveniently by making use of the Xilinx iMPACT programming software which is part of the Xilinx ISE WebPack / Design Suite.

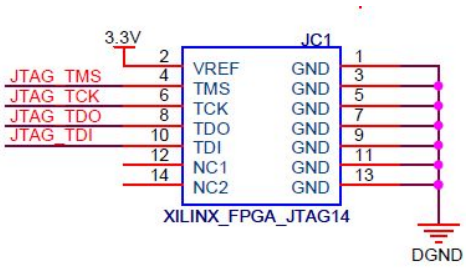

Figure 5: JTAG Connectivity on Base Board

4 Appendix A

4.1 ZingSom2 Module connector Pinout

FPGA Pin	Signal	Connector Pin		Signal	FPGA Pin
-	VCC_IN	1	2	DGND	
-	VCC_IN	3	4	B34_MC_P0	U18
-	VCC_IN	5	6	B34_MC_N0	U19
-	VCC_IN	7	8	DGND	
-	VCC_IN	9	10	B34_SC_P0	U14
-	VCC_IN	11	12	B34_SC_N0	U15
-	PWR_EN	13	14	DGND	
-	DGND	15	16	B34_IO_P8	V12
W18	B34_IO_P0	17	18	B34_IO_N8	W13
W19	B34_IO_N0	19	20	DGND	
	DGND	21	22	B34_IO_P9	U13
V20	B34_IO_P1	23	24	B34_IO_N9	V13
W20	B34_IO_N1	25	26	DGND	
	DGND	27	28	B34_IO_P10	V15
T20	B34_IO_P2	29	30	B34_IO_N10	W15
U20	B34_IO_N2	31	32	DGND	
	DGND	33	34	B34_IO_P11	V16
T11	B34_IO_P3	35	36	B34_IO_N11	W16
T10	B34_IO_N3	37	38	DGND	
	DGND	39	40	PWR_GOOD	
	1.35V	41	42	1.0V	
N18	B34_MC_P1	43	44	B34_IO_P12	T12
P19	B34_MC_N1	45	46	B34_IO_N12	U12
	DGND	47	48	B34_IO_P13	T14
N20	B34_SC_P1	49	50	B34_IO_N13	T15
P20	B34_SC_N1	51	52	DGND	
	VCCO_B34	53	54	B34_IO_P14	V17
W14	B34_IO_P4	55	56	B34_IO_N14	V18
Y14	B34_IO_N4	57	58	B34_IO_P15	T17
Y16	B34_IO_P5	59	60	B34_IO_N15	R18
Y17	B34_IO_N5	61	62	VCCO_B34	
	DGND	63	64	B34_IO_P16	T16
Y18	B34_IO_P6	65	66	B34_IO_N16	U17
Y19	B34_IO_N6	67	68	B34_IO_P17	N17
P14	B34_IO_P7	69	70	B34_IO_N17	P18
R14	B34_IO_N7	71	72	DGND	

	VCCO_B34	73	74	B34_IO_P18	R16
L19	B35_IO_P0	75	76	B34_IO_N18	R17
L20	B35_IO_N0	77	78	B34_IO_P19	P15
N15	B35_IO_P1	79	80	B34_IO_N19	P16
N16	B35_IO_N1	81	82	VCCO_B35	
	DGND	83	84	B35_IO_P10	M14
K17	B35_MC_P0	85	86	B35_IO_N10	M15
K18	B35_MC_N0	87	88	DGND	
	1.8V	89	90	B35_IO_P11	K14
M19	B35_IO_P2	91	92	B35_IO_N11	J14
M20	B35_IO_N2	93	94	1.8V	
	DGND	95	96	B35_IO_P12	H15
M17	B35_IO_P3	97	98	B35_IO_N12	G15
M18	B35_IO_N3	99	100	DGND	
	1.8V	101	102	B35_IO_P13	L14
L16	B35_SC_P0	103	104	B35_IO_N13	L15
L17	B35_SC_N0	105	106	1.8V	
	DGND	107	108	B35_IO_P14	K16
J20	B35_IO_P4	109	110	B35_IO_N14	J16
H20	B35_IO_N4	111	112	B35_MC_P1	H16
G17	B35_IO_P5	113	114	B35_MC_N1	H17
G18	B35_IO_N5	115	116	DGND	
	VCCO_B35	117	118	B35_IO_P15	F19
K19	B35_IO_P6	119	120	B35_IO_N15	F20
J19	B35_IO_N6	121	122	B35_IO_P16	E18
G19	B35_IO_P7	123	124	B35_IO_N16	E19
G20	B35_IO_N7	125	126	VCCO_B35	
	DGND	127	128	B35_SC_P1	J18
C20	B35_IO_P8	129	130	B35_SC_N1	H18
B20	B35_IO_N8	131	132	B35_IO_P17	F16
B19	B35_IO_P9	133	134	B35_IO_N17	F17
A20	B35_IO_N9	135	136	DGND	
	VCCO_MIO	137	138	B35_IO_P18	D19
	IO_MIO42	139	140	B35_IO_N18	D20
	IO_MIO40	141	142	B35_IO_P19	E17
	IO_MIO50	143	144	B35_IO_N19	D18
	IO_MIO44	145	146	VCCO_MIO	
	DGND	147	148	IO_MIO49	
	IO_MIO51	149	150	IO_MIO48	
	IO_MIO47	151	152	IO_MIO46	
	IO_MIO45	153	154	IO_MIO41	
	IO_MIO43	155	156	DGND	
	DGND	157	158	JTAG_TCK	

	USB_DP	159	160	JTAG_TDI	
	USB_DM	161	162	JTAG_TMS	
	USB_VBUS	163	164	JTAG_TDO	
	USB_ID	165	166	USB_CPEN	
	DGND	167	168	XADC_VP	
	PHY_MDI3_N	169	170	XADC_VN	
	PHY_MDI3_P	171	172	DGND	
	PHY_LED0	173	174		
	PHY_LED1	175	176		
	PHY_MDI2_N	177	178		
	PHY_MDI2_P	179	180	DGND	
	1.8V_FILT	181	182	NAND_RD	
	PHY_MDI1_N	183	184	NAND_WE	
	PHY_MDI1_P	185	186	NAND_D2	
		187	188	NAND_D0	
		189	190	NAND_D1	
	PHY_MDI0_N	191	192	PS_SRST#	
	PHY_MDI0_P	193	194	FPGA_DONE	
	DGND	195	196	PS_POR#	
	3.3V	197	198		
	3.3V	199	200	FPGA_VBATT	